Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1 (Currently Amended). An electronic circuit comprising:

a first source circuit for generating a first signal and for generating a first calibration signal responsive to a calibration mode;

a second source circuit of generating a second signal and for generating a second calibration signal responsive to the calibration mode;

a variable delay circuit for detecting a delay between said first and second calibration signals and applying a delay to said first signal responsive to the detected delay prior to passing said first signal to a third circuit receiving both the first signal and the second signal, such that the variable delay circuit accounts for all relative delays between said first and second source circuits.

2 (Original). The electronic circuit of claim 1 and further comprising a fixed delay buffer for applying a fixed delay to said second signal to compensate for delays attributable to said variable delay circuit.

3 (Original). The electronic circuit of claim 1 wherein said variable delay circuit comprises a chain of fixed delay buffers and circuitry for selecting an output of one of said fixed delay buffers responsive to the detected delay.

4 (Original). The electronic circuit of claim 3 wherein said selecting circuitry comprises circuitry for detecting a transition of said first calibration signal in said chain of fixed delay buffers responsive to an active transition of said second calibration signal.

5 (Original). The electronic circuit of claim 4 wherein said circuitry for detecting a transition comprises a plurality of flip-flops for storing outputs of respective fixed delay buffers responsive to said active transition of said second calibration signal.

6 (Currently Amended). An method of reducing skew between a first signal from a first source circuit and a second signal from a second source circuit, comprising the steps of:

generating a first calibration signal at the first source circuit responsive to a calibration mode;

generating a second calibration signal at the second source circuit responsive to the calibration mode;

detecting a best fit delay between said first and second calibration signals , such that the best fit delay accounts for all relative delays between said first and second source circuits; and

passing said first signal to a third circuit after applying the best fit delay to said first signal.

7 (Currently Amended). The method of claim 6 and further comprising the step of applying a fixed delay to said second signal to compensate for delays attributable to said passing step and passing the second signal to a third circuit after applying the fixed delay.

8 (Original). The method of claim 6 wherein said detecting step comprises the steps of:

propagating the first calibration signal through a chain of fixed delay buffers; and

detecting a transition of the first calibration signal between adjacent fixed delay buffers.

9 (Original). The method of claim 8 wherein said detecting step further comprises the step of storing outputs of the fixed delay buffers in respective flip-flops.

10 (Original). The method of claim 8 wherein said passing step comprises the step of passing the output of one of said adjacent fixed delay buffers.